Thin-film III-V solar cells using epitaxial lift-off

G.J. Bauhuis, P. Mulder and J.J. Schermer

Abstract Epitaxial lift-off is used to create thin-film III-V solar cells without sacrificing the GaAs wafer. It is based on selective etching of an AlAs release layer between the wafer and the cell structure using an HF solution. The wafer can be reused for subsequent deposition runs thereby reducing the cost of the cells. The thin-film cell can be transferred to any new carrier, e.g. glass, plastic, silicon or metal foil. Although epitaxial lift-off was first demonstrated in 1978, it took until the 1990s to make significant progress in understanding the process and devising new ways to increase the etch rate. The first single-junction epitaxial lift-off cells were made in 1996. Thin-film cells offer new cell applications based on their flexibility, low weight and possibility to deposit the cell structure in reverse order. Today the world record for single-junction cells is held by a thin-film GaAs cell, whose performance is partly based on the increased photonrecycling factor in cells with a backcontact acting as a mirror. Also state of the art tandem and inverted metamorphic thin-film cells have been demonstrated.

Keywords Epitaxial lift-off · thin-film · III-V solar cell · photonrecycling · inverted metamorphic

G.J. Bauhuis
Radboud University Nijmegen, Institute for Molecules and Materials, Heyendaalseweg 135,
6525 AJ Nijmegen, the Netherlands
e-mail: g.bauhuis@science.ru.nl

P. Mulder
Radboud University Nijmegen, Institute for Molecules and Materials, Heyendaalseweg 135,
6525 AJ Nijmegen, the Netherlands
e-mail: p.mulder@science.ru.nl

J.J. Schermer
Radboud University Nijmegen, Institute for Molecules and Materials, Heyendaalseweg 135,
6525 AJ Nijmegen, the Netherlands
e-mail: j.schermer@science.ru.nl

1 Introduction

III-V solar cells are usually not referred to as thin-film cells, because the cell structures are deposited on relatively thick GaAs or Ge wafers in order to obtain high quality single crystalline material. These materials are direct band gap semiconductors with high absorption coefficients, therefore a thickness of only a few micrometers is sufficient to absorb the light that the cell can convert into electricity. In the present wafer-based fabrication techniques, the cell structure and the wafer are processed together to a thick solar cell. The wafers are expensive (about \$100 for a 4 inch diameter GaAs wafer) and determine a significant part of the cost of III-V cells. Therefore it makes sense to separate the cell structure from the wafer. This leaves a thin-film structure, that can be transferred to a low cost foreign carrier, and the wafer which, after reconditioning, can be reused for the deposition of the next cell structure. Currently, the most mature technique to do this is Epitaxial Lift-off (ELO) where the separation is done by selective wet etching of a thin release layer between cell structure and wafer. ELO is based on the extremely high etching selectivity of $>10^6$ [1,2] for an $\text{Al}_x\text{Ga}_{1-x}\text{As}$ ($x>0.6$) release layer clad between GaAs layers in an aqueous HF solution. In fig.1 schematic presentations of the wafer-based and thin-film production processes are shown.

Fig. 1 Schematic representation of the production process for wafer-based III-V cells (left) and thin-film cells using epitaxial lift-off with the potential of substrate reuse (right).

Apart from the cost aspect, thin-film III-V cells have a number of benefits with respect to wafer-based cells, i.e. low weight, flexibility, different cell concepts as the inverted metamorphic cell [3] where the cell structure is deposited in inverse order. In the third paragraph of this chapter a more extensive overview of the thin-film cell properties will be given.

In 1978 the first attempts to separate devices from a GaAs substrate were described by Konegai et al. [4] using the so-called Peeled Film Technology. A wax layer was applied to support the circa 30 μm thick, LPE grown, fragile thin-film during the etching of a 5 μm thick release layer. After this first attempt, the method was abandoned for a long time because the lateral etch rate was too low to be of any practical use. Almost a decade later, it was noted that if the film structures have a thickness in the range of a few micrometers, the tension induced by the wax support layer causes the III/V film to curl up as it becomes undercut [5]. This was concluded to be beneficial for removal of the etch products during the process. The release layer thickness was reduced to the 10-100 nm range. As a result the lateral etch rate of the now named Epitaxial Lift-off process was raised to about 0.3 mm/h [6]. Using this process many GaAs but also InP based devices such as photodiodes [7,8], LEDs [9,10], lasers [11,12], HEMTs [13] and FETs [14] transferred to silicon, sapphire and glass plates were demonstrated. However, the process still suffered from some severe limitations. First of all the etch rate was fairly low. As a result the demonstrated devices were generally limited to several millimetres in size. ELO was typically performed by preparing the samples with wax and submerging them in the HF solution until the thin-films were found floating in the solution which could, depending on size, take up to several days. Secondly the tension induced by the wax could not be controlled well, which made it difficult to improve the process. For industrial utilisation it was essential to obtain a better control over the technique so that the process could be optimized for the separation of large area devices at sufficiently high etch rates. With this goal in mind the work on ELO at the Radboud University Nijmegen was started in the mid 1990s. An ELO setup was developed to allow for a systematic investigation on the basic parameters that determine the etch rate [3,15,16,17,18,19] and a model to describe the process was developed [20,21]. By making some essential modifications to the original ELO method, like the use of a temporary flexible carrier and applying a controlled force to allow the etchant to reach the etch front, the etch rate increased by more than a factor of 100 to rates well above 30 mm/h [16,19,21]. The ELO method has evolved to a process capable of separating layer structures from entire wafers (fig.2). Conventional photolithography techniques and wet chemical etching can be used to process the thin-film into a cell, with no loss in material quality or efficiency.

Fig. 2 Epitaxial lift-off of wafer sized thin-film structures. Upper picture a 2 inch GaAs wafer and thin-film structure on a flexible carrier after ELO. Picture below three thin-film structures retrieved from a single 4 inch Ge wafer.

2 The Epitaxial lift-off process

The basis of the Epitaxial Lift-Off process is the application of a thin, typically 10 nm, $\text{Al}_x\text{Ga}_{1-x}\text{As}$ (with $x > 0.6$, mostly x is taken as 1) release layer deposited on the wafer before the actual III-V cell structure. Since AlGaAs has a lattice constant that is almost identical to GaAs, only a minimal additional lattice misfit strain is introduced and the perfect crystal structure of the wafer can be maintained. During the ELO process the release layer is removed by wet chemical etching in an HF solution, while keeping the cell structure free of damage. It is essential to force the crevice open to allow transport of reaction products to and from the etch front. Using a wax support layer makes it difficult to control the parame-

ters that determine the etch rate. At the Radboud University Nijmegen a weight-induced epitaxial lift-off (WI-ELO) process was developed to investigate the etch mechanism and study the process parameters. In the WI-ELO setup an HF resistant temporary carrier is mounted on top of the epilayer structure. This carrier, typically a plastic foil, provides continuous support and allows for manipulation of the thin film during and after the lift-off process. A weight attached to the foil is used as a controllable external force to the film to open the crevice with a radius of curvature R .

Fig. 3 Setup used for the weight-induced epitaxial lift-off process with plastic container, pump and temperature controlled HF reservoir. This setup can be used for 4 samples in parallel. On the right a detail of a support rod with small area sample, foil, weight and HF supply probe. The setup is shown with the samples in mounting position above the container. After mounting the four samples are simultaneously lowered in the container and the etch process is started.

A process was developed in which the sample with the carrier is mounted upside down in a closed container (see fig.3 and 4a) [15,16]. In the initial set-up, a saturated vapour is created by the HF solution in the container. Under these conditions one droplet of etch solution positioned on the plastic foil against the edge of the sample on the side of the weight is generally sufficient to separate the epitaxial film from its substrate. In a later stage, the setup was modified to supply fresh etchant to the etch front at all times by a continuous flow of HF solution in order to maintain a constant etch rate. A disadvantage of this setup is that if the lift-off proceeds, the foil easily bends too much. This frequently results in cracking of the epitaxial layer structure in the final part of the process. For this reason a setup was developed in which the slit is forced open with a constant radius of curvature by guiding the foil and the part of the film that is separated over a curved surface (see fig. 4b). The size of the curved surface can easily be scaled-up to adapt for different wafer diameters. The process was demonstrated for 2 and 4 inch wafers (see

fig.2) but there is no fundamental limitation to scale-up the process towards larger wafers.

Fig. 4 Schematic representation of the ELO process: (a) WI-ELO setup with a weight attached to the foil, (b) wheel setup for a constant radius of curvature.

The reaction of AlAs with an aqueous HF solution is complex. In a systematic study the solid, aqueous and gaseous reaction products of the etch process in the absence of transport limitations were examined by a number of techniques [20]. It was found that aluminium fluoride, both in solid form as well as in solution, and arsine gas are formed. Also oxygen related species like AsO^+ , AsOH^- and AsO_2^+ were detected indicating that solid arsenic is oxidated as an intermediate step in the reaction. The etching chemistry can be described by a set of overall reactions given by:

with $n = 0, 1, 2, 3$. If the etch process takes place in the ELO geometry (i.e. through a narrow crevice) transport limitations have to be taken into account. The fact that the ELO process can be maintained with a constant high etch rate over a long period of time if the crevice is bended open, indicates that the reaction products with a relatively low solubility are at least removed a sufficient distance away from the etch front before they eventually are re-deposited at the walls of the crevice (see fig.5a). AFM surface analysis of the substrate and thin-film after ELO confirm the re-deposition of material during the process (see fig.5b) [21]. Initially the deposits were suspected to be mainly $\text{AlF}_3 \cdot \text{H}_2\text{O}$, but in a later stage SIMS analyses indicated that solid arsenic is a major compound in the re-deposited material [55]. This explains the fact that we were never able to detect gaseous AsH_3 during ELO processing. Furthermore it is found that the presence of oxygen in the etching environment accelerates the etching process, while under the same conditions a total

absence of oxygen resulted in the process coming to a halt [19]. This seems to indicate that without oxygen the re-deposition of solid arsenic more easily results in total blocking of the etch front while oxygen by removing arsenic as As_2O_3 prevents or undoes this blocking mechanism allowing the ELO process to continue.

Fig. 5 (a) Schematic representation of the situation during the ELO process where reaction products are deposited on the thin-film and the substrate surfaces, (b) AFM image of the substrate surface side after lift-off. The scale is given in micrometers.

3.1 Key process parameters

For the application of ELO the process needs to have a sufficiently high etch rate. It is and always will be a relatively slow process. With an etch rate of less than 1 mm/hour it initially took more than a day to lift-off a 2 inch diameter thin-film structure. Therefore an important goal was to speed up the process to a time scale of hours for lifting of a 4 inch thin-film, which is in the same order as the deposition time of the solar cell layer structures by MOCVD. To understand the chemistry and how the relevant parameters influence the etch rate, a diffusion and reaction related model (DR model) was developed based on the notion that the overall etch rate V_e is determined by both the diffusion of HF to the etch front and its subsequent reaction with the AlAs release layer [21]. According to this model V_e is given by:

$$V_e = \frac{[HF]}{R_d + R_r} \quad (2)$$

with $[HF]$ the HF concentration in the bulk of the solution and $R_d + R_r$ the resistance of the etch process related to diffusion and the reaction chemistry. The resistances can be expressed as:

$$R_d = \frac{\pi\sqrt{Rh^3}[AlAs]}{\sqrt{2}D_0} e^{-\frac{E_{a,d}}{kT}} \quad (3)$$

$$\text{and} \quad R_r = \frac{1}{A} e^{-\frac{E_{a,r}}{kT}} \quad (4)$$

With h the release layer thickness, R the radius of curvature, $[AlAs]$ the molar concentration of solid AlAs, D_0 the diffusion coefficient, $E_{a,d}$ the activation energy for the diffusion of HF, T the temperature, A the Arrhenius constant and $E_{a,r}$ the activation energy for the surface reaction. The WI-ELO setup was used to verify the model by determining the influence of some of the ELO process parameters on V_e . It was found that the DR model yields etch rates which are in quantitative agreement with those obtained experimentally.

The linear dependence of V_e on the HF concentration was found experimentally for $[HF] < 15$ mol/kg. For higher concentration V_e saturates, which indicates that the ELO process is limited in some way not accounted for by the DR model. The most likely explanation is that the exchange of molecules to the etch front is hindered by an insufficient effective opening of the slit.

Fig. 6 Lateral etch rate as a function of the phosphorus fraction in the $AlAs_{1-y}P_y$ release layer.

The etch rate is reaction-rate related by the dependence on the composition of the release layer. Because the lattice constant of AlAs is slightly higher than that of GaAs, there is a small negative in-plane strain ε present on the release layer. By adding small amounts of phosphores this strain can be varied. For 10 nm thick $AlAs_{1-y}P_y$ release layers, the etch rate was determined for y between 0 and 8%.

The results shown in fig.6 indicate a maximum V_e for $y=2\%$ at a small compressive strain, with a 30% gain in etch rate with respect to AIs ($y=0$).

The release layer thickness influences the diffusion limited etch rate. At a fixed temperature and radius of curvature,

$$V_e = \frac{\alpha}{\sqrt{h+\beta}} \quad (5)$$

with α and β being constants. As shown in fig.7a this relationship is valid if h is not too low. In the range between 5 and 10 nm the etch process slows down, if h is decreased further the etch process comes to a halt.

The radius of curvature R determines the opening angle of the crevice. R was varied by applying different weights to the carrier [16]. The dependence of the etch rate on R is described by the sum of a constant and a term with $V_e \sim R^{-0.5}$. V_e increases as R is reduced. However, an increased curvature involves a higher risk of breaking the single crystal ELO films so care should be taken with the optimisation of this parameter.

From the relationships 2, 3 and 4, it can be deduced that the etch rate increases exponentially with process temperature:

$$V_e = V_{e,0} e^{-\frac{E_a}{kT}} \quad (6)$$

For $h=10$ nm, V_e is raised by a factor of 5 if the temperature is increased from room temperature to 70 °C (fig.7b). For practical reasons T is limited to 100 °C and might best be kept at a value between 50-60 °C.

Fig. 7 Lateral etch rate in 20% HF solution as a function of (a) layer thickness and (b) process temperature.

Other parameters that have been investigated as strain applied to the wafer during the lift-off process [17], n- or p-type doping levels in the release layer [3], aluminium fraction x (must be >0.6) in the Al_xGaAs release layer [3], the addition of a surfactant or anti-foaming agent [22] do not influence the etch rate to the same extent.

In summary, it can be concluded that for optimized practically applicable settings an etch rate exceeding 30 mm/hr is feasible, resulting in a lift-off time of around 3 hours for a 4 inch wafer.

3.2 ELO methods for small area devices

Alternative approaches for ELO are directed to the production of microchips using a transfer-printing technique to peel and print a large number of small thin-film structures onto glass or plastic [23]. The layer stack for this method is identical to other ELO methods: a device structure that is grown over an AlAs release layer, only in this approach the AlAs layer is much thicker (1 μm) than generally applied for the full area lift-off. In this method not the entire wafer area is lifted off, but small area device structures. To do this, before lift-off the material is separated into square blocks by vertical etching through the device structure to enable exposure of the release layer to HF by immersion. Each individual device is then transfer printed one at a time, in a step and repeat fashion, onto the carrier.

An interesting feature of the transfer print method is that several device structures separated by release layers can be deposited in a single growth run and released one by one. This technique has been demonstrated for a trilayer assembly with single-junction GaAs solar cells. The cells show a slight decrease in performance from the top to the bottom cell, which is attributed to Zn diffusion. Yoon et al. [23] calculated a reduction in the cell's growth cost of about 50% for a stack of 10 cell structures. A serious drawback of this method is the small device area ($<0.5\text{mm}^2$). Such small cells can be applied for CPV, but are less suited for large area (space) panels.

Another small area lift-off approach developed by Horng et al. [24] is the use of cross-shaped pattern array to provide the etch path for the HF. After the cross-shaped holes are etched, a 50 μm thick nickel layer covering only the device areas is applied by electroplating. The nickel is attracted by a magnet to decrease the etch time during etching in an HF bath and acts as the thin-film carrier after lift-off. In this way, an entire wafer-sized thin-film structure is lifted-off simultaneously. The individual devices can be separated afterwards. The lateral etch rate decreases with increasing cell area (between 1x1 and 5x5 mm), but is always below 1 mm/hr.

3 Epitaxial lift-off cells

Conventional triple junction cells grown on Ge have their limitations. They are inflexible, brittle and relatively heavy. Therefore wafer-based cells require some kind of structural support to prevent damage. Thin-film III-V cells produced with the ELO technique offer new opportunities for device design, based on the fact that the thin-film carrier can be selected on its material properties rather than crystal growth demands. Fig.8 shows an example of flexible thin-film cells with a metal backing. Substrate reuse and thus lower cell cost has been the main driver for the development of ELO thin-film cells, but apart from this there are many interesting new concepts and applications which are not possible for wafer-based cells.

Fig. 8 Flexible ELO thin-film cells with a metal foil backing.

3.1 Thin-film III-V cell development

The first good quality thin-film III-V cell, a 4 cm² GaAs cell with a 23.3% efficiency, was made by Kopin in 1990 [25] at a time when the best wafer-based GaAs cell performance was 25.1%. The thin-film was not lifted off chemically like in ELO but mechanically using the CLEFT (Cleavage of Lateral Epitaxial Films for Transfer) technique [26]. The cell was used in a mechanical tandem in combination with CIS bottom cell. The total efficiency was 25.8% which made it the best mechanically stacked tandem cell at that time intended for use in space. No progress in CLEFT was reported after 1990.

The first cell results for ELO GaAs cells were presented in 1996 [27,28]. Lee et al. used the tension in the wax to produce small thin-film cells transferred to glass substrates after lift-off. Metallization and mesa etching were done prior to lift-off with both top and bottom contacts on the front side of the cell. The cell showed good open circuit voltage V_{oc} and short circuit current J_{sc} values, but a relatively

low FF due to a high series resistance. In the same year, using the large area lift-off approach, research at Radboud University Nijmegen showed a thin-film cell that also had proper V_{oc} and J_{sc} values, but with an even lower FF [28,29]. The efficiency was around 10%, compared to 24% for a wafer based cell with a similar layer structure. Metallisation for this thin-film cell was done after lift-off, with a full area back contact. Normally the cells undergo an anneal treatment at 450°C to reduce the contact resistance between metal contact and semiconductor. This was not possible for the thin film on the new host substrate, because of the differences in expansion coefficient between III-V material and the carrier, resulting in the cell's low FF . Another problem was the choice for $Al_{0.85}GaAs$ as the window material in the cell structure. The window is then also attacked by the HF during the lift-off, which required protection layers on the side walls that had to be removed afterwards. Also, as can be seen in fig.9 wiring of the cell was not done by bonding but with a conductive paste. Notwithstanding these imperfections which indicated that new approaches were required for several steps in the cell processing, the quality of the lifted-off material proved to be excellent showing the potential of the method. Gradually solutions were found to improve processing of the thin-film cell on a foreign carrier up to the level of a record single-junction thin-film cell with an efficiency of 24.5% in 2006 [30].

Fig. 9 One of the first operational ELO cells produced at Radboud University (left) and the first ELO cell reaching a thin-film cell record efficiency of 24.5% in 2006 (right).

Fig.9 shows the visual improvements made from the first cell to this first record cell. Further tuning of the cell structure resulted in an equal 26.1% record efficiency for a single junction GaAs cell in a regular wafer-based structure as well as in the thin-film configuration in 2009 [30]. This irrefutably demonstrates that the material quality is not affected by the ELO process. The thin-film cell used a back reflecting mirror and a reduced base thickness, but with a value of 1.045 V the potential raise in open-circuit voltage was not fully realized (see paragraph 3.3 of this chapter). Recently, Alta Devices demonstrated a thin-film GaAs cell with a

V_{oc} of 1.122 V and an efficiency of 28.8% [31,32,33], which is the highest single-junction cell efficiency up to now. ELO GaAs thin-film cells produced by several other groups confirm that there is no loss in material quality or cell efficiency after epitaxial lift-off [23,34,35,36,37].

From a lift-off perspective, multi-junction cell structures only differ from single-junction GaAs cells in their higher thickness. This increased thickness can slow down the etch rate somewhat and thus increase the lift-off time, but this is normally not a problem. It was noticed that the InGaP etching behaviour for thin-films is not the same as for material on the wafer [38]. Therefore in the processing of the thin-film cells other etchants than HCl are preferred. Excellent ELO multi-junction cells were produced by several groups including tandem cells [39,40] and IMM cells [41].

3.2 Low power to weight ratio/flexibility

For space solar cells high efficiency, high radiation resistance, a low weight and flexibility are the desired features. Because of their highest power output wafer-based III-V cells have been dominant over other cell types since the late 1990s. Wafer-based cells are mounted on a rigid honeycomb structure to prevent the wafers from breaking, resulting in relatively high weight. A thin-film cell on a flexible host substrate does not require a rigid panel assembly. This introduces new low weight options for panel design. In the past, other attempts were made for thin-film space cells which used a-Si or CIGS materials. In Japan, the experiences with these thin-films have already been used to develop lightweight solar panels containing III-V cell solar sheets from dual-junction solar cells [42]. A panel containing several sheets is unfolded using a pantographic structure. The power of the panel is 100 W/kg, compared to 50-70 W/kg for a typical rigid panel. Another example of thin-film solar cells in space applications, where PV modules can be folded and rolled is given by Farah [43].

The cells flexibility and low weight in combination with a high cell efficiency can also be used for terrestrial applications, especially if portable power is required. For example, a 10.25x15.5 inch panel with 30 single-junction GaAs thin-film cells was tested for application as battery charging device for the military [44]. The panels, with the cells laminated between two sheets of transparent fluoropolymer film, have an efficiency of 19.6% which is considerably higher than the currently used 7.8% CIGS panels.

3.3 New device designs

Wafer-based cells have a full area back contact. A thin-film cell allows access to the backside of the device. This makes it possible to apply a metal grid on front and back side. In this design the cell can be used as a bifacial cell [45] where illumination takes place from both top and bottom side using a relatively cheap mirror setup.

Such a cell can also be applied as semi-transparent cell for mechanical stacking on a lower bandgap cell. An example is a thin-film InGaP cell combined with a Si cell [46] or an InGaAsP/InGaAs tandem cell grown on InP combined with a GaAs cell [47]. In fig.10 an InGaP and GaAs semi-transparent cell are shown. The InGaP cell is illuminated from the bottom, which is the reason for the red color coming from the transmitted photons with a wavelength above 650 nm.

Fig. 10 Examples of thin-film cell designs: semi-transparent InGaP cell (left) and bifacial GaAs cell (right).

In a thin-film cell with a full area back contact the metal (mostly gold or silver) also serves as a mirror for non-absorbed photons. This doubles the optical thickness of the cell, so half of the wafer-based cell thickness is sufficient to absorb the light [48]. Using the reflectivity of the metal mirror, the thin-film cell can be designed to take advantage of the so-called photon recycling effect. This effect was already described in 1977 by Asbeck [49] and was experimentally confirmed by the very high photoluminescence lifetimes measured in GaAs layers cladded by AlGaAs [50]. Photons emitted through radiative recombination in the active layers are confined within the cell and likely to be re-absorbed. Effectively, the minority carrier lifetime in the base layer is raised potentially by one order of magnitude [51]. The recycled photons are emitted isotropically, in order to be re-absorbed with a high yield they have to be reflected on the back side by the metal mirror and on the front side by the large difference in refractive index between the III-V material

and air. Only $1/4n^2$ (2% for GaAs) of the recycled photons escapes on the front side [31], whereas the reflectivity of a gold or silver mirror on GaAs can be as high as 94-96%. For optimal light trapping, loss mechanisms as interface recombination at the window/emitter or BSF/base interface, absorption in the contact layers and non-radiative recombination in the active layers and at the perimeter must be kept as low as possible. In good quality GaAs, bulk non-radiative recombination is much lower than the radiative recombination. Perimeter recombination (non-radiative) can become a significant fraction of the total recombination for small area cells.

The saturation current density J_0 of a thin-film cell is given by [51]:

$$J_0 = q \frac{n_i^2}{N_A} W \left[\frac{1}{\tau_{nr}} + \frac{1}{\phi \tau_r} + \frac{S}{W} \right] \quad (7)$$

where N_a is the base carrier concentration, W is the width of the base layer, ϕ is the photon recycling factor, τ is the (radiative or non-radiative) lifetime and S is the recombination velocity at the base-BSF heterointerface. Assuming $\tau_{nr} \gg \phi \tau_r$ and $\phi=10$ a value of 2×10^{-21} A/cm² for J_0 is calculated for a GaAs cell. Using a realistic short circuit current of 29 mA/cm², an open circuit voltage of 1.15 V can be calculated from

$$V_{oc} = \frac{kT}{q} \left[\ln \left(\frac{J_{sc}}{J_0} + 1 \right) \right] \quad (8)$$

Calculations done by Miller et al. [31] based on the Shockley-Queisser limit also indicate that V_{oc} will be close to 1.15 V for a thin-film cell with a 100% mirror reflectivity. For a wafer-based GaAs cell they calculated a maximum V_{oc} of 1.08 V. This difference between thin-film and wafer-based cells is confirmed by the experimentally obtained best V_{oc} values for GaAs cells: 1.122 V [32] and 1.038 V [30], respectively. The best single junction thin-film cell currently has an efficiency of 28.8% [32] compared to 26.4% for a cell on the wafer [52]. Therefore, by applying a high-quality mirror on the back of a thin-film cell, the GaAs single-junction cell efficiency can be increased by 9% (relative) with respect to a wafer based-cell.

Current state of the art III-V cells are 3-junction cells consisting of the active materials InGaP, (In)GaAs and Ge (fig.11a). These cells are limited in efficiency by the Ge bottom cell, which, with 0.7 eV has a lower bandgap than desired. Future cells will likely feature 4, 5 or even 6 junctions in order to increase the efficiency to values above 45% under concentration [53]. This is not possible with only lattice matched materials grown on GaAs or Ge. An example of a new multijunction approach initiated by NREL [1,54] is the inverted metamorphic (IMM) cell where

graded buffer layers are used to alter the lattice constant to accommodate the growth of InGaAs subcell material with a 1.0 eV bandgap. The InGaP and GaAs subcells with the lattice constant of the substrate are grown first. Then gradually the lattice constant is increased, as shown schematically in fig.11b, using a graded buffer. Finally, the InGaAs subcell is grown with the new lattice constant. The cell structure is grown in inverse order, and this implies that after growth the wafer and cell structure need to be separated to facilitate use of the cell in the “sunny side up” direction (fig.11b). The epitaxial lift-off process can be used for this separation. IMM cells have been demonstrated with efficiencies of 40.8% (AM1.5, 326 suns concentration) for 3-junction [28] and 32.0% (AM0, 1 sun) for 4-junction cells [55] and have the potential for further increase in number of junctions and efficiency.

Fig. 11 Schematics of (a) conventional 3-junction cell on wafer and (b) 3-junction IMM cell where epitaxial lift-off is used to separate the cell structure from the wafer. The high bandgap subcells (InGaP and GaAs) are deposited lattice matched followed by the metamorphic InGaAs subcell.

4 Substrate reuse

One of the aims of ELO is to allow multiple reuse of the wafer after lift-off to reduce cell cost. Ideally, a minimum of wafer re-preparation between consecutive

lift-offs is required. However, exposure to the HF solution increases the surface roughness of the wafer on a nanometer scale. The roughness is about 0.3 nm for new so-called epi-ready wafers and between 2 and 4 nm for wafers that have been subjected to a 20% HF solution for 21 hours. In addition during ELO reaction residues are left on the surface [56], mainly elemental arsenic. During storage of the etched wafer under ambient conditions, from this arsenic As_2O_3 particles are formed. As a consequence of surface roughening and contamination, a re-preparation of the surface is necessary before the wafer is again suited for growth of a cell structure.

The easiest method of preparation is the application of a polishing etch solution to reduce the surface roughness of the wafer after ELO. The smoothest surface is obtained using an ammonia-peroxide solution. A wafer subjected to 21 hours in HF appears clean and smooth to the naked eye after exposure to the polishing etchant and the roughness is reduced to 0.4 nm [57]. Is this sufficient for wafer reuse for solar cells? In fig.12 the IV-curves of two GaAs cells from the same reused wafer are shown together with the curve from a thin-film cell grown a new wafer. Clearly, chemical polishing with only ammonia-peroxide results in a serious deterioration of the cell performance and a non-uniformity over the wafer. The conclusion can only be that this procedure does not sufficiently remove all surface contamination that is left after ELO.

Fig. 12 IV-curves of thin-film GaAs solar cells lifted-off from new and reused substrates. The wafers that have been treated with a polishing etchant show a clear degradation in performance, whereas the chemo-mechanically treated wafers show identical performance to cells from new wafers.

A second reclaim method is to subject the wafers to a procedure that includes a mechanical polishing step which is also used in the fabrication of epi-ready GaAs

wafers as purchased from a commercial wafer vendor. In this process first any surface contamination is removed, followed by a chemo-mechanical planarisation process to polish the surface. The minimum thickness loss of the GaAs wafer is about 10 μm , so multiple reuse of a wafer is viable. This reclaim process is commercially available at a price which is typically in the order of 15-20% of the regular price for new GaAs wafers. It has been demonstrated [57] that with chemo-mechanical polishing of the wafers a series of consecutive thin-film solar cells without any reduction in cell performance can be produced (see fig.12).

A third option is the use of protection layers deposited on the wafer before the release layer in order to avoid direct contact between the HF etchant and the wafer surface. After lift-off the protection layers can be selectively removed by wet chemical etching before the wafer is loaded into the reactor chamber. Lee et al. [58] have subjected a wafer with protection layers on top to an HF solution for 48 hours to simulate the ELO process. They found a similar roughness for the surface after etching of the protection layers as for a new wafer. Cells grown on these two types of wafers showed an identical performance. Horng et al. [24] produced single-junction wafer-based GaAs cells on recycled wafers that were used for ELO up to four times. After each ELO step the protection layers were chemically etched and a new ELO structure consisting of protection layers, release layer and a 3 μm thick GaAs layer, was grown. The performance of the cells decreased to below 90% of the initial performance when the substrate was reused more than twice. This is attributed to an increase in the diode saturation current I_0 caused by a lower material quality of the grown crystal. Both these papers show results of wafer-based cells on reused wafers. Up to now, good quality ELO thin-film cells grown on reused wafers with protection layers have not been demonstrated.

5 Future perspectives

With today's record efficiency of 44.0% under a concentration of 942 suns [38] III-V solar cells have not reached their full potential. The multi-junction concept has the perspective of obtaining efficiencies above 45% and maybe even 50% under concentration. New designs for cells with more than 3 junctions require the use of thin-film cells in some form [27,59,60] either as a free standing thin-film cell or in combination with cells grown on different wafer materials through a layer transfer process.

A basic method for obtaining a thin-film cell by etching/polishing of the wafer after growth is widely used [1,28,29], but this is an expensive method because the wafer, which has a large contribution in the total cell cost, is lost. Epitaxial lift-off offers the possibility of wafer reuse and is more and more maturing after being under investigation for more than 20 years, resulting in good quality cells and a

stable process. Other options, i.e. the controlled spalling technology [61,62], are still in its infancy.

In the last five years, companies like Alta Devices [63] and Microlink Devices [26,50,52,54] have developed a wafer-scale, epitaxial lift-off manufacturing process and are currently in pilot production. Activities in Europe are also initiated (tf2 devices). The transfer printing technique is adopted by Semprius to produce cells for CPV [64]. These commercial activities show the potential of ELO as a production method for III-V thin-film cells. The application of thin-film cells offers new opportunities. In space cells the flexibility and low weight can lead to different design of the panels of which the first concepts have already been developed [24,25]. For terrestrial purposes these high-efficiency cells are initially used for mobile systems where the thin-film properties like low weight, non-brittleness, and flexibility can be exploited. Examples are unmanned aerial vehicles (UAVs), military applications as charging tents and backpacks, and consumer electronics (mobile phones). In a later stage wide scale application in CPV or flat panel PV can be expected.

References

1. Wu, X.S., Coldren, L.A., Merz, J.L.: Selective etching characteristics of HF for Al_xGa_{1-x}As/GaAs. *Electron. Lett.* **21**, 558-559 (1985).
2. Voncken, M.M.A.J., Schermer, J.J., Bauhuis, G.J., Mulder, P., Larsen, P.K.: Multiple release layer study of the intrinsic lateral etch rate of the epitaxial lift-off process. *Appl. Phys. A* **79**, 1801-1807 (2004).
3. Geisz, J.F., Kurtz, Sarah, Wanlass, M.W., Ward, J.S., Duda, A., Friedman, D.J., McMahon, W.E., Moriarty, T.E., Kiehl, J.T.: High-efficiency GaInP/GaAs/InGaAs triple-junction solar cells grown inverted with a metamorphic bottom junction. *Appl. Phys. Lett.* **91**, 023502 (2007).
4. Konagai, M., Sugimoto, M., Takahashi, K.: High efficiency GaAs thin film solar cells by peeled film technology. *J. Cryst. Growth* **45**, 277-280 (1978).
5. Yablonovitch, E., Gmitter, T., Harbison, J.P., Bhat, R.: Extreme selectivity in the lift-off of epitaxial GaAs films. *Appl. Phys. Lett.* **51**, 2222-2224 (1987).
6. Yablonovitch, E., Hwang, D.M., Gmitter, T.J., Florez, L.T., Harbison, J.P.: Van der Waals bonding of epitaxial liftoff films onto arbitrary substrates. *Appl. Phys. Lett.* **56**, 2419-2421 (1990).
7. Schumacher, H., Gmitter, T.J., LeBlanc, H.P., Bhat, R., Yablonovitch, E., Koza, M.A.: High-speed InP/GaInAs photodiode on sapphire substrate. *Electron. Lett.* **25**, 1653-1654 (1989).
8. Kobayashi, F., Sekiguchi, Y.: GaAs Schottky photodiode fabricated on glass substrate using epitaxial lift-off technique. *Jpn. J. Appl. Phys.* **31**, L850-L852 (1992).
9. Schnitzer, I., Yablonovitch, E., Caneau, C., Gmitter, T.J., Scherer, A.: 30% external quantum efficiency from surface textured thin-film, light emitting diodes. *Appl. Phys. Lett.* **63**, 2174-2176 (1993).
10. Sasaki, Y., Katayama, K., Koishi, T., Shibahara, K., Yokoyama, S., Miyazaki, S., Hirose, M.: High speed GaAs epitaxial lift-off and bonding with high alignment accuracy using a sapphire plate. *J. Electrochem. Soc.* **146**, 710-712 (1999).

11. Yablonovitch, E., Kapon, E., Gmitter, T.J., Yun, C.P., Bhat, R.: Double heterostructure GaAs/AlGaAs thin film diode lasers on glass substrates. *IEEE Photon. Technol. Lett.* **1**, 41-42 (1989).
12. Pollentier, I., Buydens, L., Van Daele, P., Demeester, P.: Fabrication of a GaAs-AlGaAs GRIN-SCH SQW laser diode on silicon by epitaxial lift-off. *IEEE Photon. Technol. Lett.* **3**, 115-117 (1991).
13. Shah, D.M., Chan, W.K., Caneau, C., Gmitter, T.J., Song, J.-I., Hong, B.P., Micelli, P.F., De Rosa, F.: Epitaxial lift-off GaAs HEMT's. *IEEE Trans. Electron Devices* **42**, 1877-1881 (1995).
14. Morf, T., Biber, C., Bächtold, W.: Effects of epitaxial lift-off on the DC, RF and thermal properties of MESFET's on various host materials. *IEEE Trans. Electron Devices* **45**, 1407-1413 (1998).
15. Schermer, J.J., Bauhuis, G.J., Mulder, P., Meulemeesters, W.J., Haverkamp, E., Voncken, M.M.A.J., Larsen, P.K.: High rate epitaxial lift-off of InGaP films from GaAs substrates. *Appl. Phys. Lett.* **76**, 2131-2133 (2000).
16. Voncken, M.M.A.J., Schermer, J.J., Maduro, G., Bauhuis, G.J., Mulder, P., Larsen, P.K.: Influence of radius of curvature on the lateral etch rate of the weight induced epitaxial lift-off process. *Mat. Sci. Eng. B* **95**, 242-248 (2002).
17. Voncken, M.M.A.J., Schermer, J.J., Bauhuis, G.J., Van Niftrik, A.T.J., Larsen, P.K.: Strain-accelerated etching of AlAs for epitaxial lift-off. *J. Phys.: Condens. Matter* **16**, 3585-3596 (2004).
18. Van Niftrik, A.T.J., Schermer, J.J., Bauhuis, G.J., Van Deelen, J., Mulder, P., Larsen, P.K.: The influence of $\text{In}_x\text{Ga}_{1-x}\text{As}$ and $\text{GaAs}_{1-y}\text{Py}$ layers surrounding the AlAs release layer in the epitaxial lift-off process. *Crystal Growth & Design* **7**, 2472-2480 (2007).
19. Van Niftrik, A.T.J., Schermer, J.J., Bauhuis, G.J., Mulder, P., Larsen, P.K., Van Setten, M.J., Attema, J.J., Tan, N.C.G., Kelly, J.J.: The role of HF species and dissolved oxygen on the epitaxial lift-off process of GaAs using AlAsP release layers. *J. Electrochem. Soc.* **155**, D35-D39 (2008).
20. Voncken, M.M.A.J., Schermer, J.J., Van Niftrik, A.T.J., Bauhuis, G.J., Mulder, P., Larsen, P.K., Peters, T.P.J., De Bruin, B., Klaassen, A., Kelly, J.J.: Etching AlAs with HF for epitaxial lift-off applications. *J. Electrochem. Soc.* **151**, G346-G351 (2004).
21. Van Niftrik, A.T.J., Schermer, J.J., Bauhuis, G.J., Mulder, P., Larsen, P.K., Kelly, J.J.: A diffusion and reaction related model of the epitaxial lift-off process. *J. Electrochem. Soc.* **154**, D629-635 (2007).
22. Maeda, J., Sasaki, Y., Dietz, N., Shibahara, K., Yokoyama, S., Miyazaka, S., Hirose, M.: High-rate GaAs epitaxial lift-off technique for optoelectronic integrated circuits. *Jpn. J. Appl. Phys.* **36**, 1554-1557 (1997).
23. Yoon, J., Sungjin, J., Chun, I.S., Jung, I., Kim, H.-S., Meitl, M., Menard, E., Li, X., Coleman, J.J., Paik, U., Rogers, J.A.: GaAs photovoltaics and optoelectronics using releasable multilayer epitaxial assemblies. *Nature* **465**, 329-334 (2010).
24. Horng, R.H., Tseng, M.C., Wu, F.L., Li, C.H., Wu, C.H., Yang, M.D.: Thin film solar cells fabricated using cross-shaped pattern epilayer lift-off technology for substrate recycling applications. *IEEE Trans. El. Dev.* **59**, 666-672 (2012).
25. Gale, R.P., McClelland, R.W., King, B.D., Gormley, J.V.: High-efficiency thin-film AlGaAs-GaAs double heterostructure solar cells. In: *Proceedings of 20th IEEE Photovoltaic Specialists Conference*, pp. 446-450 (1988).
26. McClelland, R.W., Bozler, C.O., Fan, J.C.C.: A technique for producing epitaxial films on reusable substrates. *Appl. Phys. Lett.* **37**, 560-562 (1980).
27. Lee, X.Y., Verma, A.K., Wu, C.Q., Goertemiller, M., Yablonovitch, E.: Thin film GaAs solar cells on glass substrates by epitaxial liftoff. In: *Proceedings of 25th IEEE Photovoltaic Specialists Conference*, pp.53-55 (1996).

28. Hageman, P.R., Bauhuis, G.J., Van Geelen, A., Van Rijsingen, P.C., Schermer, J.J., Giling, L.J.: Large area, thin film epitaxial lift off III/V solar cells. In: Proceedings of 25th IEEE Photovoltaic Specialists Conference, pp.57-60 (1996).
29. Van Geelen, A., Hageman, P.R., Bauhuis, G.J., Van Rijsingen, P.C., Schmidt, P., Giling, L.J.: Epitaxial lift-off GaAs solar cell from a reusable GaAs substrate. *Mat. Sci. Eng. B* **45**, 162-171 (1997).
30. Bauhuis, G.J., Mulder, P., Haverkamp, E.J., Huijben, J.C.C.M., Schermer, J.J.: 26.1% thin-film GaAs solar cell using epitaxial lift-off. *Sol. En. Mat. Sol. Cells* **94**, 1314-1318 (2009).
31. Miller, O.D., Yablonovitch, E., Kurtz, S.R.: Strong internal and external luminescence as solar cells approach the Shockley-Queisser limit. *IEEE J. Photovolt.* **2**, 303-311 (2012).
32. Green, M.A., Emery, K., Hishikawa, Y., Warta, W., Dunlop, E.D.: Solar cell efficiency tables (version 41). *Progr. Photovolt.* **21**, 1-11 (2013).
33. Kayes, B.M., Nie, H., Twist, R., Spruytte, S.G., Reinhardt, F., Kizilyalli, I.C., Higashi, G.S.: 27.6% conversion efficiency, a new record for single-junction solar cells under 1 sun illumination. In: Proceedings of 36th IEEE Photovoltaic Specialists Conference, pp.4-8 (2011).
34. Taguschi, H., Soga, T., Jimbo, T.: Epitaxial lift-off process for GaAs solar cell on Si substrate. *Sol. En. Mat. Sol. Cells* **85**, 85-89 (2005).
35. Tseng, M-C, Horng, R-H, Wu, F-L, Wu, C-H, Yang, M-D.: Performance of GaAs/Mirror/Cu-substrate thin-film solar cells. *IEEE Trans. Electr. Dev.* **58**, 3898-3904 (2011).
36. Omnes, F., Guillaume, J.C., Nataf, G., Jäger-Waldau, G., Vennegues, P., Gibart, P.: Substrate free GaAs photovoltaic cells on Pd-coated silicon with a 20% AM1.5 efficiency. *IEEE Trans. Electr. Dev.* **43**, 1806-1811 (1996).
37. Tatavarti, R., Dzankovic, A., Martin, G., Tuminello, F., Navaratnarajah, R., Du, G., Vu, D.P., Pan, N.: Lightweight, low cost GaAs solar cells on 4" epitaxial liftoff (ELO) wafers. In: Proceedings of 33th IEEE Photovoltaic Specialists Conference, pp.1-4 (2008).
38. Van Deelen, J., Mulder, P., Bauhuis, G.J., Van Niftrik, A.T.J., Haverkamp, E.J., Schermer, J.J., Larsen, P.K.: Study of wet chemical etching of $\text{Al}_x\text{Ga}_{1-x}\text{InP}_2$ films using hydrochloric acid. *J. Electrochem. Soc.* **153**, C442-C448 (2006).
39. Tatavarti, R., Hillier, G., Martin, G., Wibowo, A., Navaratnarajah, R., Tuminello, F., Hertkorn, D., Disabb, M., Youtsey, C., McCallum, D., Pan, N.: Lightweight, low cost In-GaP/GaAs dual-junction solar cells on 100 mm epitaxial liftoff (ELO) wafers. In: Proceedings of 34th IEEE Photovoltaic Specialists Conference, pp.2065-2067 (2009).
40. Bauhuis, G.J., Mulder, P., Haverkamp, E.J., Schermer, J.J., Nash, L.J., Fulgoni, D.J.F., Ballard, I.M., Duggan, G.: Inverted thin film InGaP/GaAs tandem solar cells for CPV applications using epitaxial lift off. In: Proceedings of 35th IEEE Photovoltaic Specialists Conference, pp.1243-1247 (2010).
41. Tatavarti, R., Wibowo, A., Elarde, F., Tuminello, F., Pastor, R., Giannopoulos, T., Osowski, M., Chan, C., Youtsey, C., Hillier, G., Pan, N.: Large area, epitaxial lift-off, inverted metamorphic solar cells. In: Proceedings of 36th IEEE Photovoltaic Specialists Conference, pp.1941-1944 (2011).
42. Shimazaki, K., Kobayashi, Y., Takahashi, M., Imaizumi, M., Takamoto, T., Ito, T., Nozaki, Y.: Progress in development of ultra-lightweight solar panel using space solar sheet. In: Proceedings of 35th IEEE Photovoltaic Specialists Conference, pp. 725-730 (2010).
43. Farah, J.: Dry-epitaxial lift-off, integration, interconnect and encapsulation of foldable/rollable high efficiency solar cell modules. In: Proceedings of 37th IEEE Photovoltaic Specialists Conference, (2012).
44. Trautz, K.M., Jenkins, P.P., Walters, R.J., Scheiman, D., Hoheisel, R., Tatavarti, R., Chan, R., Miyamoto, H., Adams, J.G.J., Elarde, V.C., Grimsley, J.: Mobile solar power. *IEEE J. Photovolt.* **3**, 535-541 (2013).

45. Schermer, J.J., Bauhuis, G.J., Mulder, P., Haverkamp, E.J., Van Deelen, J., Van Niftrik, A.T.J., Larsen, P.K.: Photon confinement in high-efficiency, thin-film III-V solar cells obtained by epitaxial lift-off. *Thin Solid Films* **511-512**, 645-653 (2006).
46. Schermer, J.J., Mulder, P., Bauhuis, G.J., Voncken, M.M.A.J., Van Deelen, J., Haverkamp, E., Larsen, P.K.: Epitaxial lift-off for large area thin film III/V devices. *Phys. Stat. Sol. A* **202**, 501-508 (2005).
47. Hanappel, T., Sagol, B.E., Seidel, U., Szabo, N., Schwarzburg, K., Bauhuis, G.J., Mulder, P.: Measurement of an InGaAsP/InGaAs tandem solar cell under GaAs. In: *Proceedings of 33th IEEE Photovoltaic Specialists Conference*, pp. 1-3 (2008).
48. Bauhuis, G.J., Schermer, J.J., Mulder, P., Voncken, M.M.A.J., Larsen, P.K.: Thin film GaAs solar cells with increased quantum efficiency due to light reflection. *Sol. En. Mat. Sol. Cells* **83**, 81-90 (2004).
49. Asbeck, P.: Self-absorption effects on the radiative lifetime in GaAs-AlGaAs double heterostructures. *J. Appl. Phys.* **48**, 820-822 (1977).
50. Ahrenkiel, R.K., Dunlavy, D.J., Keyes, B., Vernon, S.M., Dixon, T.M., Tobin, S.P., Miller, K.L., Hayes, R.E.: Ultralong minority-carrier lifetime epitaxial GaAs by photon recycling. *Appl. Phys. Lett.* **55**, 1088-1090 (1989).
51. Lush, G., Lundstrom, M.: Thin film approaches for high-efficiency III-V cells. *Solar Cells* **30**, 337-344 (1991).
52. Green, M.A., Emery, K., Hishikawa, Y., Warta, W., Dunlop, E.D.: Solar cell efficiency tables (version 36). *Prog. Photovolt.* **16**, 346-352 (2010).
53. Law, D.C., King, R.R., Yoon, H., Archer, M.J., Boca, A., Fetzer, C.M., Mesropian, S., Isshiki, T., Haddad, M., Edmondson, K.M., Bhusari, D., Yen, J., Sherif, R.A., Atwater, H.A., Karam, N.H.: Future technology pathways of terrestrial III-V multijunction solar cells for concentrator photovoltaic systems. *Sol. En. Mat. Sol. Cells* **94**, 1314-1318 (2010).
54. Geisz, J.F., Friedman, D.J., Ward, J.S., Duda, A., Olavarria, W.J., Moriarty, T.E., Kiehl, J.T., Romero, M.J., Norman, A.G., Jones, K.M.: 40.8% efficient inverted triple-junction solar cell with two independently metamorphic junctions. *Appl. Phys. Lett.* **93**, 123505 (2008).
55. Stan, M., Aiken, D., Cho, B., Cornfeld, A., Diaz, J., Ley, V., Korostyshevsky, A., Patel, P., Sharps, P., Varghese, T.: Very high efficiency triple junction solar cells grown by MOVPE. *J. Cryst. Growth* **310**, 5204-5208 (2008).
56. Smeenk, N.J., Engel, J., Mulder, P., Bauhuis, G.J., Bissels, G.M.M.W., Schermer, J.J., Vlieg, E., Kelly, J.J.: Arsenic formation on GaAs during etching in HF solutions: relevance for the epitaxial lift-off process. *ECS J Solid State Sci. Techn.* **2**, P58-P65 (2013).
57. Bauhuis, G.J., Mulder, P., Haverkamp, E.J., Schermer, J.J., Bongers, E., Oomen, G., Köstler, W., Strobl, G.: Wafer reuse for repeated growth of III-V solar cells. *Prog. Photovolt.* **18**, 155-159 (2010).
58. Lee, K., Zimmerman, J.D., Xiao, X., Sun, K., Forrest, S.R.: Reuse of GaAs substrates for epitaxial lift-off by employing protection layers. *J. Appl. Phys.* **111**, 033527 (2012).
59. Cornfeld, A.B., Patel, P., Spann, J., Aiken, D., McCarthy, J.: Evolution of a 2.05 eV AlGaInP top sub-cell for 5 and 6J-IMM applications. In: *Proceedings of 38th IEEE Photovoltaic Specialists Conference*, (2012).
60. Patel, P., Aiken, D., Chumney, D., Cornfeld, A., Lin, Y., Mackos, C., McCarthy, J., Miller, N., Sharps, P., Stan, M.: Initial results of the monolithically grown six-junction inverted metamorphic multi-junction solar cell. In: *Proceedings of 38th IEEE Photovoltaic Specialists Conference*, (2012).
61. Bedell, S.W., Shahrjerdi, D., Hekmatshoar, B., Fogel, K., Lauro, P.A., Ott, J.A., Sosa, N., Sadana, D.: Kerf-less removal of Si, Ge, and III-V layers by controlled spalling to enable low-cost PV technologies. *IEEE J. Photovolt.* **2**, 141-147 (2012).

62. Shahrjerdi, D., Bedell, S.W., Ebert, C., Bayram, C., Hekmatshoar, B., Fogel, K., Lauro, P., Gaynes, M., Gokmen, T., Ott, J.A., Sadana, D.K.: High-efficiency thin-film InGaP/InGaAs/Ge tandem solar cells enabled by controlled spalling technology. *Appl. Phys. Lett.* **100**, 053901 (2012).
63. Mattos, L.S., Scully, S.R., Syfu, M., Olson, E., Yang, L., Ling, C., Kayes, B.M., He, G.: New module efficiency record: 23.5% under 1-sun illumination using thin-film single-junction GaAs solar cells. In: *Proceedings of 37th IEEE Photovoltaic Specialists Conference*, pp. 3187-3190 (2011).
64. Furman, B., Menard, E., Gray, A., Meitl, M., Bonafede, S., Kneeburg, D., Ghosal, K., Bukovnik, R., Wagner, W., Gabriel, J., Seel, S., Burroughs, S.: A high concentration photovoltaic module utilizing micro-transfer printing and surface mount technology. In: *Proceedings of 37th IEEE Photovoltaic Specialists Conference*, pp. 475-480 (2011).